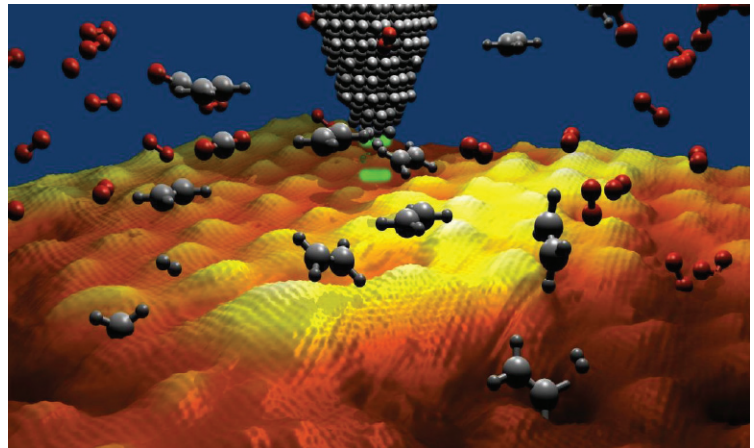# SPM Open Source Controller Model Mk2-A810

This DSP-based system has been specially designed to meet the Scanning Probe Microscopy (SPM) application requirements. The SPM Open Source Controller offers:

- 8 analog I/O capable of operating at up to 150 kHz with a +-10V dynamic range
- 2/16-bit counters inputs
- 16 individually configurable GPIOs
- Low noise and very high DC stability
- Very low input-output group-delay
- 5502 DSP from Texas Instrument running at 300 MHz
- SPARTAN 3 FPGA from Xilinx
- High Speed USB interface controller

Free complete SPM software is available at **http://gxsm.sourceforge.net**

Advanced SPM features can be implemented using the 16 individually configurable GPIOs and the two 16-bit counters. These counters are synchronized with the analog sampling and can be used as simple pulse counters or Quadrature Encoder Pulse (QEP) counters.

Based on the SR-MK2 DSP board and SR2-A810 board, the SPM Open Source Controller is a convenient rack-mount enclosure providing quality connectors and wiring to ensure the best S/N ratio.

With all these features , the kit SR2-A810 + SR-Mk2 has the best performance/price ratio on the market for a SPM control system.

For more information, please consult Soft dB website at www.softdb.com or contact us by phone at **418-686-0993**, toll free at **1-866-686-0993** or by email at **contact@softdb.com**.

SPM Open Source Controller Model Mk2-A810

Soft dB

TECHNICAL DATA

Inputs:

- Resolution: 16 bits
- Sampling Rate: 11.4 Hz to 150 kHz
- Input type: Single Ended
- Dynamic range: ±5V, ±10V
- Input leakage: ±1 µA max
- Anti-aliasing filter: None
- Analog input bandwidth: 0 to 10 MHz (includes DC)
- Noise: 1 bit RMS = 150 µV RMS on ±5V range

    1 bit RMS = 300 µV RMS on ±10V range
- Group-delay: 2 samples (includes all hardware and software FIFO delay)

Outputs:

- Resolution: 16 bits
- Group-delay: between 2.5 and 3.25 samples depending on output used
- Offset drift with temp.:   ±2 ppm FSR / ºC
- Gain drift with temp.:   ±2 ppm FSR / ºC
- Offset drift with Time: ±13ppm FSR / 500 hours
- Samplig Rate: 11.4 kHz to 150 kHz
- Analog output bandwidth: 0 to >80 kHz (includes DC)
- Output type: Single Ended
- Dynamic Range: ±10V
- Noise: 20 MHz bandwidth: up to 55mV pk on 0xFFFF(-1) to 0x0000 (0) alternating code sequence.

    20 kHz bandwidth: <25µV RMS
- Source/Sink ability: 4 mA
- Anti-aliasing filter: None

GPIOs:

- Number of IOs: 16
- Configurability: All IOs individually configurable as input or output.
- IO level: 3.3V CMOS (5V-tolerant inputs)

Counters:

- Number of counters: 2
- Counter width: 16-bit (can be increased to any width in software)
- Inputs: Two Quadrature Encoder Pulse (QEP) inputs and one general-purpose pulse input per counter
- IO level: 3.3V CMOS (5V-tolerant inputs)
- Max count frequency: 50 MHz
- Min pulse width: 20 ns (to be reliably counted the high and low states on the counter inputs must be at least 20ns wide)
- Synchronism: Both counters are sampled synchronously to the ADC samples.

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